REMARKS

I. Introduction

In response to the Office Action dated March 22, 2005, Applicants have canceled claims 1, 3, 6 and 8, without prejudice or disclaimer. Claims 2, 4-5 and 9-10 have been amended so as to address the pending rejection under 35 U.S.C. § 112, second paragraph. The dependency of claims 4 and 9-10 has also been amended to depend on claim 2. No new matter has been added.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. Drawings Objection

The drawings are objected to under 37 C.F.R. §1.83(a), because the fuse, as recited in claims 6 and 8, is not shown. As claims 6 and 8 have been canceled, the objection thereto is moot.

III. The Rejection Of Claims 1-10 Under 35 U.S.C. § 112, Second Paragraph

Claims 1-10 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to provide antecedent basis. Specifically, in the statement of the rejection, the Examiner identified several perceived antecedent basis issues, which arose via minor clerical oversights. The present Amendment addresses these antecedent basis issues, thereby overcoming the stated basis for the imposed rejection. Accordingly, Applicants respectfully request that the rejection of claims 1 through 10 under the second paragraph of 35 U.S.C. §112 be withdrawn in view of the foregoing amendment.

IV. The Rejection Of Claims 1-10 Under 35 U.S.C. § 103

Claims 1-10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over USP No. 6,711,705 to Yasui. Applicants respectfully traverse this rejection for at least the following reasons.

Claim 1 recites in-part a self-diagnosis circuit, which diagnoses the memory and outputs a diagnosed result to an external power control circuit.

In the pending rejection, the Examiner reads the device power source 123 of Yasui as being provided outside of and supplying power to the memory under test MUT 19. That is, the Examiner reads the device power source 123 of Yasui as the claimed external power control circuit. However, in doing so, it is clear that the diagnosed result of the memory under test MUT 19 is ***not*** forwarded to the device power source 123. In this regard, Applicants note that the Examiner relies on the bidirectional BUS as channeling the detected result of the memory under test MUT 19 to the device power source 123. Applicants respectfully disagree with such interpretation, because Yasui discloses only that the test bus BUS is utilized to connect the main controller 111 to the components 111-113/118/120-123. However, Yasui is completely silent with regard to outputting the failure data at the failure relief analyzer 120 to the device power source 123. It should be noted that a mere connection between the main controller 111 and the device power source 123 ***cannot*** reasonably be interpreted as necessarily sending the failure data signal of the memory under test MUT 19 from the main controller 111 to the device power source 123. This is evidenced by the fact that the main controller 111 only functions to provide a starting instruction or command to the pattern generator 112 for generating pattern (see, col. 2, lines 23-25), or to cause the failure relief analyzer 120 to perform a data updating operation (see, col. 5, lines 40-42 and 53-60, and col. 6, lines 24-28). Accordingly, the main controller 111 or

the test bus BUS is incapable of sending the detected failure result of the memory under test MUT 19 from the failure relief analyzer 120 to the device power source 123. Thus, the allegation set forth in the pending Office Action that the device power source 123 "receives output from the failure relief analyzer 120 via bidirectional BUS" is not supported by and departs from the disclosure of Yasui.

Furthermore, claim 1 recites that a supply of power to the redundancy relief circuit is controlled ***independently*** of a supply of power to a semiconductor integrated circuit by a power control circuit operating ***based on*** the diagnosed result. However, as discussed *supra*, the device power source 123 does not receive the result of the memory under test MUT 19 from the failure relief analyzer 120, and therefore does not operate based on such result. Yasui is also silent with regard to controlling the power supply of the alleged redundancy relief circuit independently from the power supply of the alleged semiconductor integrated circuit.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, *Kalman v. Kimberly-Clark Corp., 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983)*, and at a minimum, Yasui fails to disclose or suggest the foregoing claim elements, it is clear that Yasui does not anticipate claim 2 or any of the claims dependent thereon.

V. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.,*

819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as independent claim 2 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

VI. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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